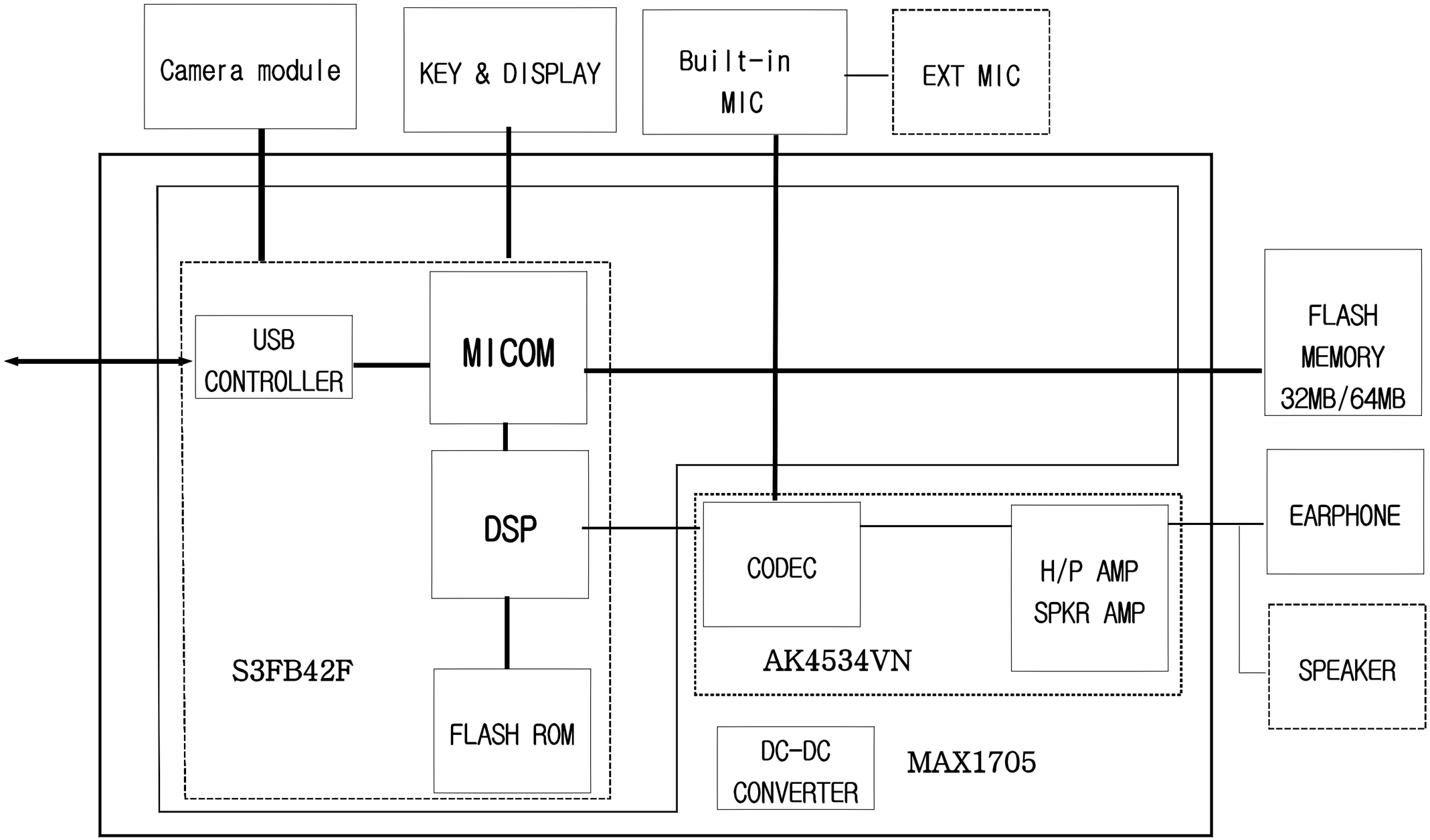
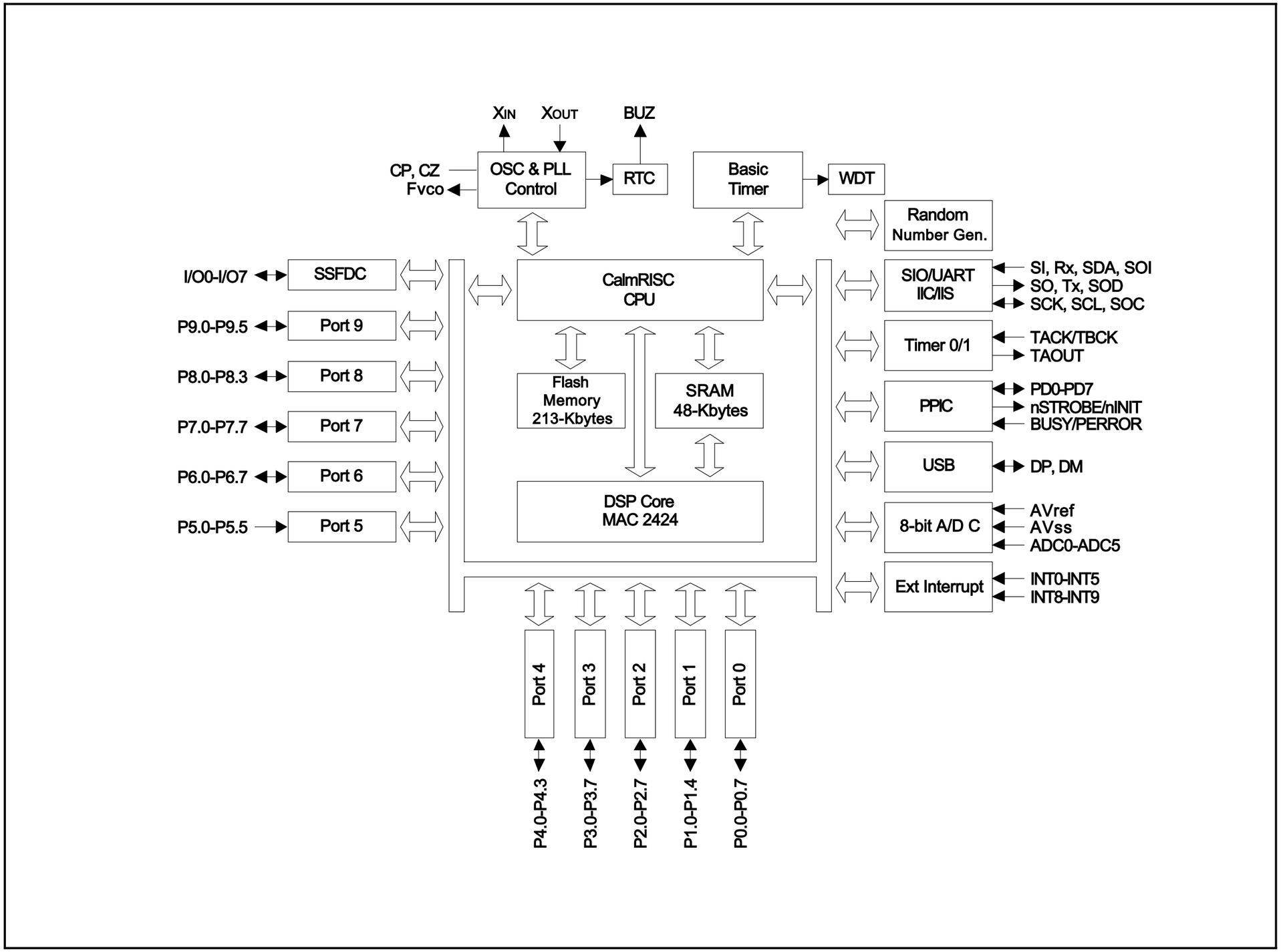
3. 계통도

3-1. TOTAL

VY-H200 Block Diagram




XIN
XOUT
BUZ
CP, CZ
Fvco
OSC & PLL Control
RTC
Basic Timer
WDT
Random Number Gen.
I/O0-I/O7
SSFDC
P9.0-P9.5
Port 9
P8.0-P8.3
Port 8
P7.0-P7.7
Port 7
P6.0-P6.7
Port 6
P5.0-P5.5
Port 5
CalmRISC CPU
Flash Memory 213-Kbytes
SRAM 48-Kbytes
DSP Core MAC 2424
SIO/UART IIC/IIS
SI, Rx, SDA, SOI
SO, Tx, SOD
SCK, SCL, SOC
Timer 0/1
TACK/TBCK
TAOUT
PPIC
PD0-PD7
nSTROBE/nINIT
BUSY/PERROR
USB
DP, DM
8-bit A/D C
AVref
AVss
ADC0-ADC5
Ext Interrupt
INT0-INT5
INT8-INT9
Port 4
Port 3
Port 2
Port 1
Port 0
P4.0-P4.3
P3.0-P3.7
P2.0-P2.7
P1.0-P1.4
P0.0-P0.7